UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,862,161 B2
DATED : March 1, 2005
INVENTOR(S) : Woo

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Title page,
Item [56], **References Cited**, insert the following:
-- OTHER PUBLICATIONS Duvvury et al., "ESD Protection: Design and Layout Issues for VLSI Circuits," IEEE Transactions on Industry Application, vol. 25 no. 1, January/February 1989, pp. 41-47.

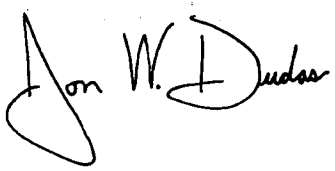
Keller, J. K., "Protection of MOS Integrated Circuits from Destruction by Electrostatic Discharge," IIT Research Institute, 1981, pp. 73-80.

Hulett, T.V., "On Chip Protection of High Density NMOS Devices," pp. 90-96.

Protective Device, at http://www.delphion.com/tdbs/tdb?&order=85A+61057, IBM Technical Disclosure Bulletin, April 1985, pp. 6814-6815. --

Signed and Sealed this

Fifth Day of July, 2005



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Director of the United States Patent and Trademark Office